DR. BABASAHEB AMBEDKAR TECHNOLOGICAL UNIVERSITY, LONERE

Regular and Supplementary Summer 2024

Course: B. Tech **Branch: Electrical Engineering and Allied** **Semester: IV**

Subject Code & Name: Analog and Digital Electronics BTBS404

Max Marks: 60 **Date: 20/06/2024** **Duration: 3 Hrs.**

Instructions to the Students:

1. *All the questions are compulsory.*
2. *Use of non-programmable scientific calculators is allowed.*
3. *Assume suitable data wherever necessary and mention it clearly.*

Marks

Q. 1 Solve Any Two of the following.

A) Explain the various operations of regions of a transistor in CE configuration on its output characteristics. **06**

B) What are different methods of transistor biasing? Explain any one in detail. **06**

C) The h parameters of a transistor used in a single stage amplifier circuit are h_{ic} = 1100, h_{rc} = 1, h_{fc} = -51, h_{oc} = 25μA. Determine the amplifier parameters for CC configuration when $R_s = R_L$ = 10 kΩ. **06**

Q.2 Solve Any Two of the following.

A) What are various characteristics of an ideal Op-Amp? Discuss in details. **06**

B) Draw the block diagram of an Op-amp and explain the purpose of using each block. **06**

C) Explain Op-Amp as a differentiator with neat circuit diagram and necessary equations. **06**

Q. 3 Solve Any Two of the following.

A) Convert the following numbers: **06**

a) $(1101101.101)_2 = (\quad ? \quad)_{10}$

b) $(126.75)_{10} = (\quad ? \quad)_8$

c) $(375.75)_{10} = (\quad ? \quad)_{16}$

B) Solve the following arithmetic operations **06**

a) Subtract $(15)_{10}$ from $(10)_{10}$ using 2's compliment method of binary subtraction.

b) Subtract $(14)_{10}$ from $(18)_{10}$ using 1's compliment method of binary subtraction.

C) Explain all logic gates with their symbols, output expression and truth table. **06**

Q.4 Solve Any Two of the following.

A) Explain TTL NAND gate circuit (Totem Pole Arrangement) with the help of circuit diagram. **06**

B) What is meant by MOS logic family? Explain working of NAND gate by NMOS logic. **06**

C) Explain J-K flip-flop with circuit diagram and truth table. **06**

Q. 5 Solve Any Two of the following.

A) Reduce the expression for f (A, B, C, D) = Σ_m (0,1,2,3,5,7,8,9,11,14) using K-map. **06**

B) Explain half adder circuit with the truth table. **06**

C) Reduce the expression for f (A, B, C, D) = πM (2,3,4,5,6,7,8,11,12) **06**

***** End *****